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10/734,132	12/15/2003	Yong Deok Cho	40296-0056	9165

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,132	CHO, YONG DEOK	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-9 and 11* is/are rejected.

7)☒ Claim(s) *2-5,10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-11 are presented for examination.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Korea on 4/17/2003. It is noted, however, that applicant has not filed a certified copy of the English translation of the application as required by 35 U.S.C. 119(b).

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 6/28/2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner has considered the information disclosure statement.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "The output signal from the NAND gate ND12 is delayed by the first delay block 51, and the strobe signal SACLK as a pulse signal is outputted ..." (page 13 lines 1-3) as described in the specification. The examiner contends that the

SACLK pulse signal in question in FIG.5 is instead delayed by the trailing edge of GIOSTP. The delay 51 mainly controls pulse width. The examiner requests that the applicant change the drawing of FIG.5 in this regard because the drawing does not depict the stated function. No new matter should be introduced.

5. For the same reason as above for FIG.5, the examiner objects to FIG.8 because the leading edge of GIOSTP does not control the pulse SACLK (rather the trailing edge controls the pulse). No new matter should be introduced.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet"

pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The abstract of the disclosure is objected to because the last line should instead recite, "... global I/O lines or a glitch generated ...".. Correction is required. See MPEP § 608.01(b).

7. The disclosure is objected to because of the following informalities:

a. Page 2 line 14 should be corrected to recite, "... an output signal ~~from~~ to the fail ...".

b. Page 9 line 6 should be corrected to recite, "... test circuit ~~test~~ tests 16 global ...".

c. Page 12 line 4 should be corrected to recite, "... an inverter ~~12~~ INV12 ...".

d. The examiner objects to the phrase on page 13 line 2-3, "The output signal from the NAND gate ND12 is delayed by the first delay block 51 ...". The drawing clearly shows that another signal is responsible for delaying the SACLK signal, and that the above phrase is incorrect. Appropriate correction is required, but no new matter should be introduced.

Claim Objections

8. Claim 1 is objected to because of the following informality: The preamble should be corrected to recite, "... wherein the test block~~s~~ ~~comprises~~ comprise: ...".

9. Claim 6 is objected to because of the following informality: The 3rd line should be corrected to recite, "... transmitting ~~an~~ a ...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112 First Paragraph

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 1, 8 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the best mode requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The applicant has incorrectly disclosed the feature (page 12), "The control block 50 serves as a corrector for initialization of the whole circuits or for stable operation on skew between the global I/O lines and on glitch generated in a logic circuit device." In the drawings

and Specification. This feature is incorrectly embodied in FIG.5 and 8 and further described on page 14 of the application in such a manner as to make it comparable to the prior art, and therefore is not an improvement thereof.

11. Claims 1, 8 and 9 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure that is not enabling. "... sampling clock signals enable memory cells to perform a stable operation on skew between global I/O lines or [a] glitch generated in internal circuits." , critical or essential to the practice of the invention, but not included in the claims is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The disclosure fails to properly describe this critical operation (see above rejection).

12. Claims 1, 8 and 9 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for strobe block 6 of the prior art (page 5 of application), does not reasonably provide enablement for "... delay block 51 delays an output signal ... for a predetermined time." (page 12 of application). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims. The delay block 51 only shapes the pulse width in question, and so the critical feature (see Abstract) of removing "glitches" is in question.

Claim Rejections - 35 USC § 112 Second Paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase on lines 5 and 6 of the claim, "... a test timing ..." is indefinite because Claim 1 also has identified "a test timing" on line 14 of the claim. The examiner is unsure whether the applicant intends the test timing in the claim to be the same one as iterated in Claim 1.

The examiner is also unsure of the meaning of the phrase, "a test timing of the test timing" in lines 5 and 6. The examiner requests clarification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

14. Claims 1 and 6-9 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art of FIG.1 and 2 and the prior art disclosure in the application, pages 1-7 (herein APA).

As per Claim 1:

The APA teaches an I/O compression test circuit for compression testing data loaded on a plurality of global I/O lines (FIG.1), comprising: a plurality of test blocks (FIG.1 1-4) for testing a plurality of global I/O line groups (FIG.1 GIO<15:0>) depending on a test enable signal (FIG.1 TMCOMP), wherein the plurality of global I/O lines are divided into the plurality of global I/O line groups (FIG.1 1-4 with outputs TBS1-4); a decision block (FIG.1 ND1, INV1, ND2, INV2, NOR1) for deciding a test result in response to output signals from the plurality of test blocks (FIG.1 TBS1-4); a driving block (FIG.1 PM1, NM1, INV3, INV4) for outputting a test result signal (FIG.1 TGIO) in response to a decision signal outputted from the decision block (FIG.1 ND2 output); and a control block (FIG.1 6) for controlling a test timing of the test blocks (FIG.1 8), initializing an input terminal of the decision block (STN is initially high just before test starts) and controlling a driving timing of the driving block (STN is driven low by the timing originated by GIOSTP).

As per Claim 6:

The APA further teaches the circuit according to claim 1, wherein the driving block comprises: a transmission means (FIG.1 PM1, NM1) for selectively transmitting a driving control signal (FIG.1 output of INV1) outputted from the decision block synchronously (FIG.1 STN uses GIOSTP for synchronization) with respect to an output signal from the control block (FIG.1 STN); and a driving means (FIG.1 INV3, INV4) for pulling up or down an output terminal (FIG.1 TGIO) in response to a signal selectively transmitted by the transmission means (by ND2 and NOR1).

As per Claim 7:

The APA further teaches the circuit according to claim 6, wherein the driving block further comprises a latch means for maintaining a potential of the output terminal (FIG.1 INV3, INV4 is a latch).

As per Claim 8:

The APA further teaches the circuit according to claim 1, wherein the control block comprises: a strobe signal generator (FIG.1 6) for generating a strobe signal (FIG.1 STN) in response to a compression test enable signal (FIG.1 TMCOMP) and a detecting signal (FIG.1 GIOSTP), wherein the strobe signal controls a test timing of the test timing (APA page 5 lines 5-10), wherein the detecting signal is activated when data are loaded on the global I/O line (APA page 4 lines 21-24; an initialization signal generator for generating an initialization signal in response to the compression test enable signal and the detecting signal (during the period before GIOSTP, the signal STN is high which serves as initialization), wherein the initialization signal initializes an input terminal of the decision block to a predetermined level (FIG.1 STN high); and a driving control signal generator (FIG.1 ND5, delay block 8) for generating a driving control signal (into delay block 8) in response to the strobe signal.

As per Claim 9:

The APA further teaches the circuit according to claim 8, wherein the strobe signal generator comprises: a logic means (FIG.1 ND5) for performing a logic operation on the compression test enable signal (FIG.1 TMCOMP) and the

detecting signal (FIG.1 GIOSTP); and a pulse generator (FIG.1 8) for outputting a pulse signal (FIG.1 STN) in response to an output signal from the logic means. As per Claim 11:

The APA further teaches the circuit according to claim 8, wherein the driving control signal generator comprises a delay means (FIG.1 delay block 8) for delaying the strobe signal.

Allowable Subject Matter

15. Claims 2-5 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: The APA teaches an I/O compression circuit that decides test results of I/O data groups to be either a pass or fail state, driving a compressed test result state based on timing as an output from the circuit. But the APA has failed to further suggest or disclose the patentable feature as is claimed in Claim 2. Specifically, the admitted prior art has failed to disclose a feature of Claim 2, namely, a first test means for outputting a first level when at least one of data transmitted into the global I/O line group is at a different level depending on an output signal from the logic means; and a second test means for outputting a second level when at least one of data transmitted into the global I/O line group is at a different level depending on an output signal from the logic means. Therefore, Claim 2, and

Claims 3-5 and 10, which are dependent on Claim 2, would be allowable as set forth above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kim et al., U.S. Patent No. 7,013,413.

Beffa et al., U.S. Patent No. RE38,956.

Fujioka et al., U.S. Patent No. 6,731,553.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

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